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Multiple Valued Logic for Synthesis and Simulation of Digital Circuits

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ABSTRACT
The Multiple valued logic(MVL) has increased attention in the last decades because of the possibility to represent the information with more than two discrete levels.Advancing from two-valued to four-valued logic provides a progressive approach. In new technologies, the most delay and power occurs in the connections between gates. When designing a function using MVL, we need fewer gates,which implies less number of connections, then less delay. In the existing system, the 4:1 multiplexer is designed using the MVL logic and various paramaters are analysed. In the proposed system, the idea of designing a Barrel shifter using the multiple valued logic and the parameters are all analyzed. All these designs are verified using Modelsim simulator.
Keywords **–** Feynman, Fredkin, Multiple valued reversible logic, Reversible Barrel shifter

I. INTRODUCTION

A Barrel shifter is the n inputs and n outputs combinational logic circuit in which k select lines controls the bit shift operation. Barrel shifter can be unidirectional allowing data to be shifted only to left (or right), or bi-directional which provides data to be rotated or shifted in both the directions. A barrel shifter having n inputs and k select lines is called (n, k) barrel shifter. Among the different designs of barrel shifter, the logarithmic barrel shifter is most widely used because of its simple design, less area and the elimination of the decoder circuitry.The n-bit Logarithmic Barrel Shifter contains log2 (n) stage where the ith stage either shifts over 2i bits or leaves the data unchanged. Each stage of a logarithmic barrel shifter is controlled by a control bit. If the control bit is set to one then the input data will be shifted in the associated stage else it remains unchanged. The proposed work presents the designs of multiple value barrel shifter.

In the existing system, the 4:1 multiplexer is designed using the MVL logic. For designing this logic, they had used the gates like eand1, eand2, eand3 and suc gates. This multiplexer works on the basis of the selection lines as the inputs. For producing outputs one selection line has given as the input instead of two selection lines. By designing the synthesis of an MVL multiplexer and latch memory circuits, based on the ICMVL gates, for illustrating the utilization of the proposed IC MVL gates for quaternary MVL is produced.

In the proposed system, the Barrel shifter using the Multiple Valued Logic is designed. This Barrel shifter has 4 inputs which is multiple valued and produces four outputs which is also multiple valued. This basically performs the shifting operation in a parallel manner which generates random data as the outputs. This shifter in turn uses the two different gates called Feynman gate and Fredkin gate. Thus the Multiple Valued Barrel shifter is designed and the parameters are analyzed for the normal shifter. Thus all these designs will be designed and verified using the Modelsim Simulator. In the proposed system, the concept is analyzed for a different gates produces less power. The overall performance of the system is good.

II. STANDARD REVERSIBLE GATES

1. INTRODUCTION:

The large number of components in modern systems on chip (SoCs) presents new challenges to designers. The high integration of different systems increases the number and length of interconnections, hence the overall complexity involving the connections of these systems. Moreover, interconnections are becoming the dominant aspect of the circuit delay for state-of-the-art circuits due to the advent of deep sub-micron technologies (DSM). This fact is becoming even more significant with each new technology generation. Interconnections play an even more crucial role in Field Programmable Gate Arrays (FPGA), because they not only dominate the delay, but they also aggressive impact power consumption and area. For FPGAs to reach a larger market, their excessive power dissipation must be severely reduced. Moreover, if one could reduce the FPGA area without losing logic capabilities, one could enhance the yield and reduce prices, or even increase the amount of memory available inside the FPGA. To reduce the area of the FPGA, a reduction in the interconnection is

mandatory, since interconnections take large amount of area. Multiple-valued logic (MVL) has received increased attention in the last decades because of the possibility to represent the information with more than two discrete levels. Representing data in a MVL system is more effective than the binary based representation, because the number of interconnections can be significantly reduced, with major impact in all design parameters: less area dedicated to interconnections; more compact and shorter interconnections, leading to increased performance; lower interconnect switched capacitance, and hence lower global power dissipation.

In new technologies the most delay and power occurs in the connections between gates. When designing a function using Multiple-Valued Logic, we need fewer gates, which implies less number of connections, then less delay. Same is true in case of software (program) realization of logic. Also, most the natural variables like color, is multi-valued, so it is better to use multi-valued logic to realize it instead of coding it into binary.

Thus, there is a need for an innovative approach in order to push the speed limit of computing. Now is the time to depart from the two-valued logic to venture into multi-valued logic and even into infinite-valued (Fuzzy) logic. Advancing from two-valued to four-valued logic provides an progressive approach. Four symbols {0, 1, 2, 3} are needed to distinguish the four values. The four values might represent anything, for example, the four bases {A, T, C, G} found in DNA, or probability {0, 1/3, 2/3, 1}. These four values can be converted to binary numbers {00, 01, 10, 11}, or they can simply represent integers {0, 1, 2, 3}. It is also possible to start from the ground up by designing components needed for constructing four-valued logic circuits. Each four-valued logic gates will operate two bits of data at a time, and each memory cell will record two bits at once. Now, each wire or CPU pin can have four states, which could double the amount of data that can be transferred between the CPU and its connected components without increasing the number of pins on the CPU.

2. Feynman Gate:

Feynman gate is a two input and two output gate. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate and Controlled NOT gate, representation is shown in figure 1.[1]

3. Fredkin Gate:

A 3*3 Fredkin gate means the three input and three output. Quantum cost of a Fredkin gate is 5. This gate can be used as a multiplexer, representation is shown in figure 2. [1]

4. MVL Barrel Shifter:

A Barrel shifter is the n inputs and n outputs combinational logic circuit in which k select lines controls the bit shift operation.

III. EQUATIONS

Feynman Gate:

The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by, [1]

- P=A . ---------- (1)
- Q=A⊕B . ---------- (2)

As shown in fig(1), table(1) respectively.

Fredkin Gate:

The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by,[1]

- P=A . ---------- (3)
- Q=A′B ⊕ AC ---------- (4)
- R=A′C ⊕ AB ---------- (5)

IV. FIGURES AND TABLES

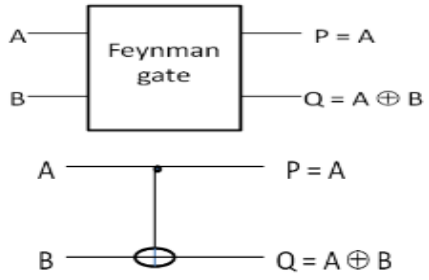


Figure 1: Feynman Gate

Table 1: Truth table of Feynman gate

A	B	C	D
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1: Truth table of Feynman gates

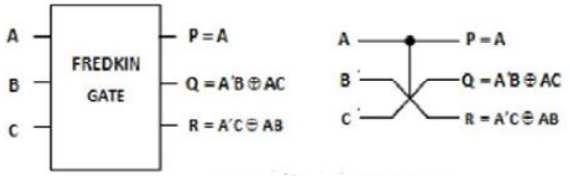


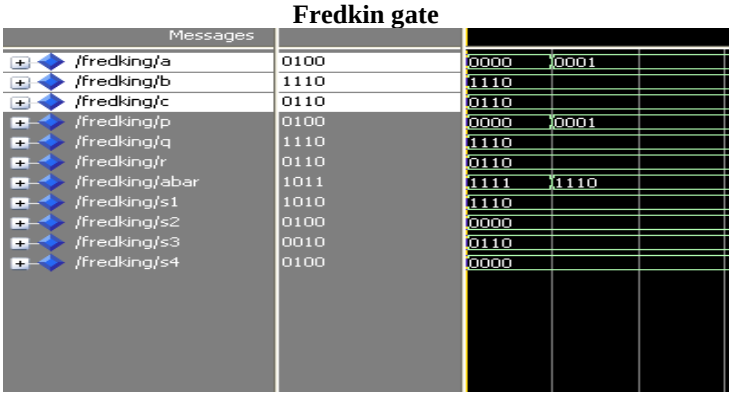
Figure 2: Fredkin Gates

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

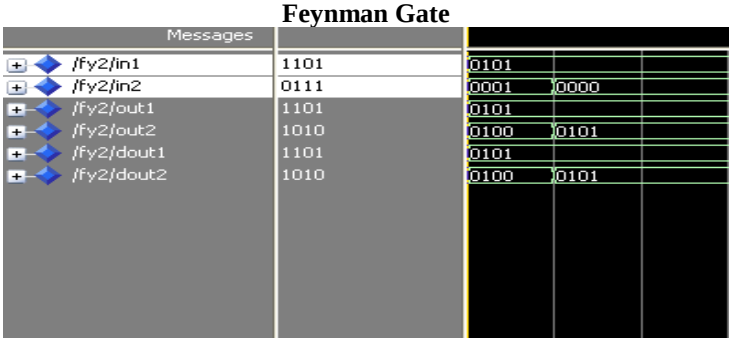
Table 2: Truth Table of Fredkin Gates

V. SIMULATION RESULTS

Fredkin gate

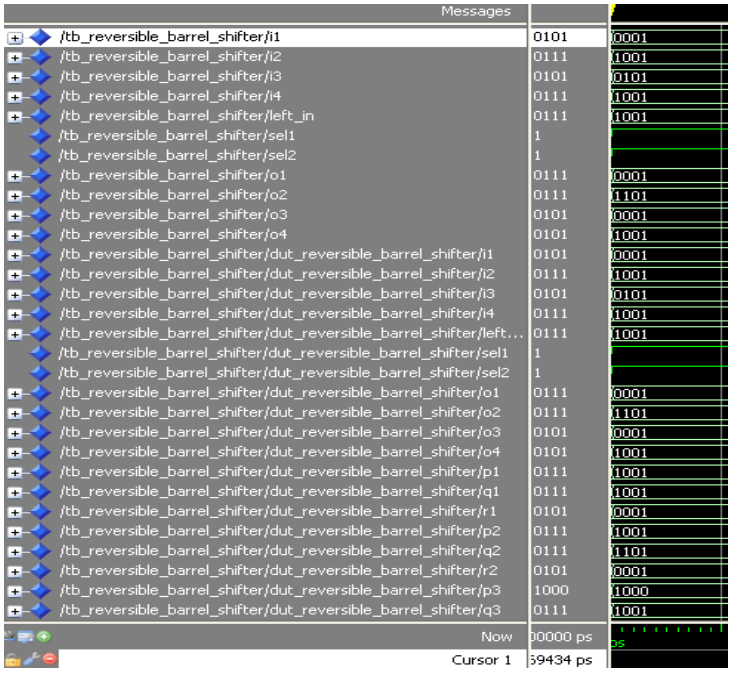


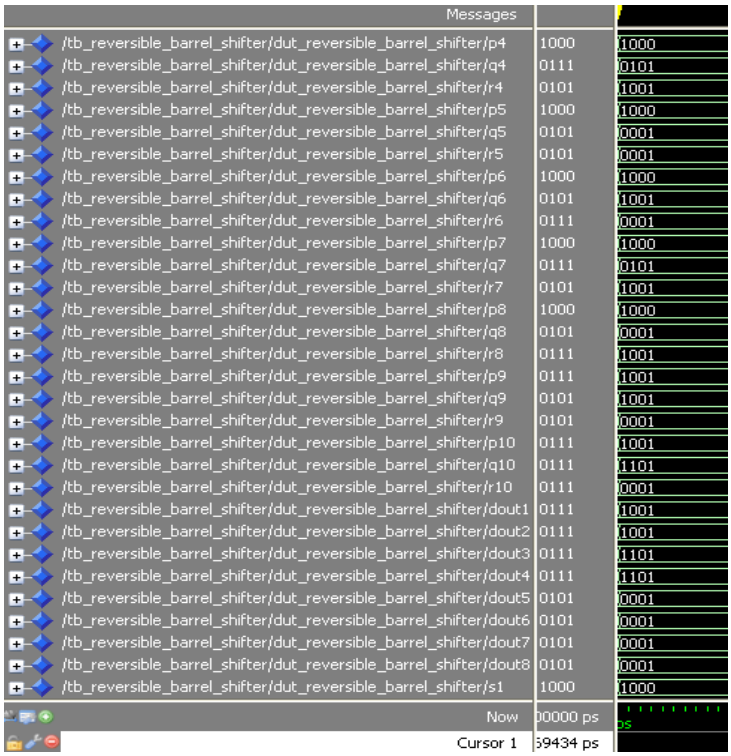
Feynman Gate



MVL BARREL SHIFTER

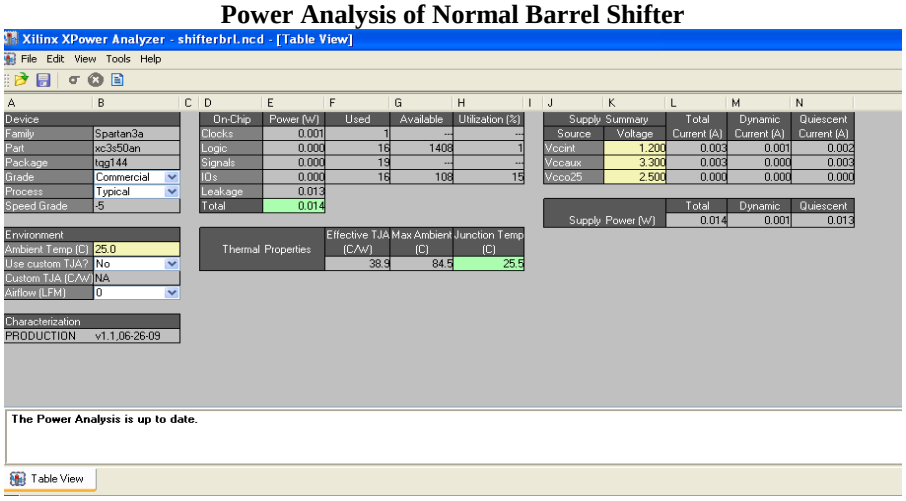
Barrel shifter is a digital circuit that can shift a data word by specified no.of bits in one clock cycle. It can be implemented as a sequence of multiplexer. The advantage of it is it takes one machine cycle only to shift n no. of values.



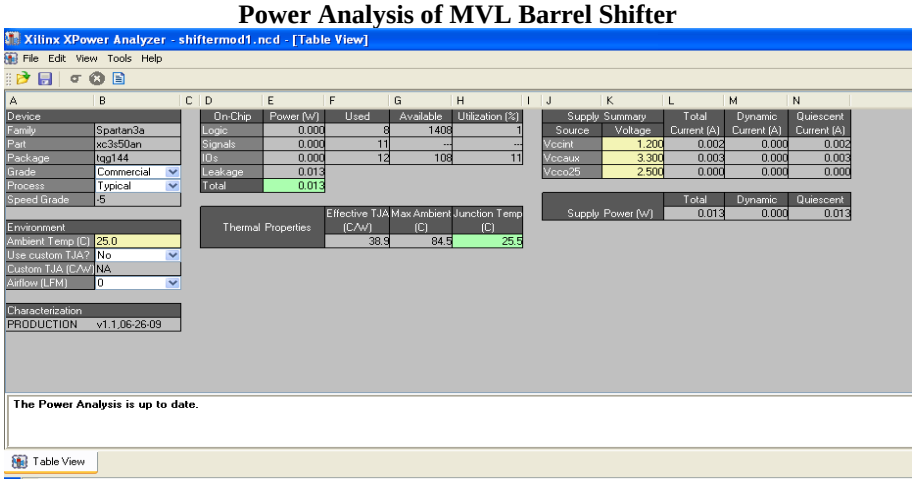


VI. HARDWARE RESULTS

Power Analysis of Normal Barrel Shifter



Power Analysis of MVL Barrel Shifter



VII. CONCLUSION

In this paper, the different gates were analyzed and designed. These gates exhibit the behavior of the controlled NOT gate and the multiplexer. This is further implemented in the design of a four bit barrel shifter which shifts incoming data and produces random output. The Barrel shifter designed works on the basis of Multiple valued logic in which the inputs and the outputs are multiple values . Thus all these designs are designed and the outputs are successfully verified using Modelsim simulator. In future, the comparison between normal barrel shifter and the newly designed MVL barrel shifter in terms of reducing power, delay and area will be shown.

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